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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEEK, JACOB M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/500,524	SUSNOW ET AL.	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/9/2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,17 and 30-35* is/are rejected.

7)☒ Claim(s) *6 - 16, 18 - 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 4, 30, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US Patent 6,028, 837) in view of IEEE Standard 802.3, 1998.

With regard to claim 1, Miller teaches a write controller with a comparator mechanism for detecting if link data contains an IDLE signal (see Figure 2, 22 and column 5, lines 9 – 23) and a "jabber" control mechanism (see column 5, line 63 – column 6 line 16). Miller is silent with respect to the details of his jabber control device, but states it is Ether Ring, which is interpreted as a variation of Ethernet and is described by IEEE Standard 802.3, 1998. IEEE 802.3 provides the details of jabber control techniques; Figure 14-5 is cited as an illustration of jabber control functionality. Non-Jabber Output block of figure 14-5 monitors DO (data out) when active, and if IDLE is detected (DO=idle where idle is defined in section 14.2.3.1), then control loop cycles back and restarts monitoring process which is interpreted by examiner as a reset of count time. Referring again to figure 14-5, when timer (counter) exceeds timeout value generates an output value (xmit_max_timer_done). IEEE 802.3 is silent on output pulse being of a single link clock cycle in duration but this would be a design choice as the digital design techniques for generating such a pulse are well known to those of ordinary skill on the art for the output of a timer expiration. IEEE 802.3, in figure 14-5, shows an output

signal (DO = active * xmit_max_timer_done) to the JAB block, where xmit is shown to be set to disable which is interpreted as a means for disabling data storage to an elastic buffer (FIFO) and is defined by a Boolean equation. It would have been obvious to one of ordinary skill in the art at the time of invention to implement a write controller for an elastic buffer for a LAN / WAN / MAN with the features claimed as the timers and jabber control mechanisms are defined in IEEE 802.3 standard as these features are required to be compatible with industry standards.

With regard to claim 3, Miller and IEEE is silent with respect to an n-bit counter being used as a timer mechanism, however the IEEE standard does specify time intervals that must be measured when assessing jabber (see section 14.10.4.5.7, items 2 & 3). Counter circuits are commonly used for the implementation of timers in digital equipment and therefore the use of an n-bit counter would have been a design choice based on the clock frequency used in the system. The DISABLE signal and IDLE are addressed by the IEEE document and the behavior described as Boolean equation, the specifics of the implementation of logic would be a design choice based on architecture of the logic device used. It would have been obvious to one of ordinary skill in the art at the time of invention to implement a write controller for an elastic buffer for a LAN / WAN / MAN with the features claimed as the timers and jabber control mechanisms are defined in IEEE 802.3 standard as these features are required to be compatible with industry standards.

With regard to claim 4, Miller and IEEE is silent with respect to comparator being a NOR gate. The DISABLE signal and IDLE are addressed by the IEEE document and the behavior described as Boolean equation, the specifics of the implementation of logic would be a design choice based on architecture of the logic device used. It would have been obvious to one of ordinary skill in the art at the time of invention to implement a write controller for an elastic

buffer for a LAN / WAN / MAN with the features claimed as the timers and jabber control mechanisms are defined in IEEE 802.3 standard as these features are required to be compatible with industry standards.

With regard to claims 30 and 32, the steps claimed as method are a restatement of the functions of specific components of the apparatus claimed above and therefore would have been obvious considering the aforementioned rejection of claims 1 and 3.

With regard to claims 34 and 35, compliance with the NGIO specification as claimed does not constitute a further limitation as any device compliant with this specification will have be compliant to the limitations cited.

2. Claims 2 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US Patent 6,028, 837) in view of IEEE Standard 802.3, 1998 in further view of Keller et al (US Patent 5,671,227).

With regard to claim 2, Miller in view of IEEE is silent with respect to the additional limitation of a 1st and 2nd comparator for the detection of 1st and 2nd idle sequences. Keller et al teach a synchronization circuit compromising multiple comparators for the recognition of various pattern sequences. It would have been obvious to one of ordinary skill in the art at the time of invention to use a pattern detector as described by Keller in order to facilitate the detection of a known pattern.

With regard to claim 31, the steps claimed as method is a restating of the functions of specific components of the apparatus claimed above and therefore would have been obvious considering the aforementioned rejection of claim 2.

3. Claims 5 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US Patent 6,028, 837) in view of IEEE Standard 802.3, 1998 in further view of Camilleri et al (US Patent 6,434,642).

With regard to claim 5, Miller in view of IEEE teaches the use of a FIFO as memory storage, but is silent with respect to the additional limitation of a succession of D-type flip-flops as part of his write controller. Camilleri et al teach a FIFO memory system containing a succession of D-type flip-flops (see Figure 2, block 210 where the address registers are D-Type flip-flops (see fig. 3). It would have been obvious to one of ordinary skill in the art at the time of invention to utilize Camilleri's invention in Miller's device to provide a FIFO with better reliability that would avoid glitches (see '642, column 3, line 9 – 16).

With regard to claim 33, the steps claimed as method is a restating of the functions of specific components of the apparatus claimed above and therefore would have been obvious considering the aforementioned rejection of claim 5.

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Patent 5,970, 069) in view of Camilleri et al (US Patent 6,434,642).

With regard to claim 17, Kumar teaches a computer network compromising a host system (see figure 2A, 30, 46, 48, 51 where these devices provide host functionality), at least one remote system (see Figure 2a, 52, 53, 51), a multi-stage switch compromising different switches (see Figure 1, 14 where the Internet / Intranet block is inherently made up of a collection of switches and routers), and an elastic buffer (see figure 23a, 254,256, and associated functional blocks and section 4.4 where buffer operation is described) provided to host adapter (see Figure 5, element 150, 152). Kumar describes that his device contains FIFO's but is silent with respect to the details of the write controller. Camilleri teaches a read controller compromised of multiple functional blocks (see Figure 1, 105, 107, 113) operating at receiver clock (see Figure 1, RCLK) for selecting read address (see figure 1, 105) to of memory (see figure 1, 101) to retrieve received data, and for inserting NOP sequences (see Figure 1, Read_Allow and Figure 6b, Read_Allow where disabling of Read_Allow signal is

interpreted as provides no-operation sequence for the duration of the disabling of Read_Allow signal. It would have been obvious to one of ordinary skill in the art at the time of invention to utilize Camilleri's invention in Kumar's device to provide a FIFO with better reliability that would avoid glitches (see '642, column 3, line 9 – 16).

Allowable Subject Matter

5. Claims 6 – 16, and 18 – 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Cited Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ancheta et al (US Patent 4,974,223) and Kinoshita et al (5,140,618) describe methods of flag (pattern) detection, which appears germane to comparator function claimed. Williams et al (US Patent 5,084,841) and Castellano (US Patent 5,555,524) disclose the use of Gray counters for FIFO control which appear germane to aspects of applicant's invention. Moorwood et al (US Patent 5,430,726) and Lohmeyer (US Patent 5,513,376) discloses devices that would appear to be related to the area of invention of the applicant and contain jabber control and FIFO functions.

Other Cited Prior Art

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM

JAYANTI PATEL
SUPERVISORY PATENT EXAMINER